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EXAMINER	
XIAO, KE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,542	LEE ET AL.	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 24 December 2008.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 5,18,20,22,27 and 32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 5,18,20,22,27 and 32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 27 is objected to because of the following informalities:

Claim 27 recites the limitation "gate driving voltage" in the last line. The examiner suggests this be changed to -- gate driving circuit --.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 18, 20, 22, 27 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) and Tsutsui (US 7,196,701).

Regarding **Claim 5**, the AAPA teach a method for supplying power to a liquid crystal display comprising steps of:

taking a power source voltage having a constant level greater than 2.9V from a power source of a system (AAPA, Fig. 2); and

supplying the power source voltage greater than 2.9V to an interface circuit, a timing controller, and a data driving circuit, and a gate driving circuit for processing digital signal (AAPA, Fig. 2 VCC elements 11-14); and

raising or reducing the power source voltage greater than 2.9V using a DC-DC converter to generate a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH, and a gate low voltage VGL (AAPA, Fig. 2 element 16), wherein the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit (AAPA, Fig. 2 element 13), and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit (AAPA, Fig. 2 element 14).

The AAPA fails to teach that the power source is less than 2.9V. Tsutsui does, however, teach a similar power source, while in the power saving mode a *constant* low level voltage is provided without variation, used for the same function that is less than 3.1V (Tsutsui, Fig. 3 element 300 and power save control signal). A person of ordinary skill in the art upon analyzing Tsutsui would have reasonably used any voltage values that are appropriate for different loads, including voltages less than 2.9V. The exact voltage values used are dependent on the voltage that is required to drive the load and are completely arbitrary, and therefore it would have been obvious to try voltages less than 2.9V along with low power loads to achieve the predictable result of power conservation. Additionally, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the power saving power supply of Tsutsui in place of the generic power supply of the AAPA in order to reduce power consumption.

Regarding **Claim 18**, the AAPA teaches an apparatus for supplying power to a liquid crystal display comprising steps of:

a power source of a system for generating a power voltage having a constant level over 2.9V (AAPA, Fig. 2); and

an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal by taking the power source voltage (AAPA, Fig. 2 elements 11-14); and

a DC-DC converter for raising or reducing the power source voltage over 2.9V using a DC-DC converter to generate a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH, and a gate low voltage VGL (AAPA, Fig. 2 element 16), wherein the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit (AAPA, Fig. 2 element 13), and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit (AAPA, Fig. 2 element 14),

wherein the power source voltage is supplied to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit.

The AAPA fails to teach that the power source is less than 2.9V. Tsutsui does, however, teaches a similar power source, while in the power saving mode a *constant* low level voltage is provided without variation, used for the same function that is less than 3.1V (Tsutsui, Fig. 3 element 300 and power save control signal). A person of ordinary skill in the art upon analyzing Tsutsui would have reasonably used any voltage values that are appropriate for different loads, including voltages less than 2.9V. The

exact voltage values used are dependent on the voltage that is required to drive the load and are completely arbitrary, and therefore it would have been obvious to try voltages less than 2.9V along with low power loads to achieve the predictable result of power conservation. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the power saving power supply of Tsutsui in place of the generic power supply of the AAPA in order to reduce power consumption.

Regarding **Claim 20**, the AAPA further teaches:

the interface circuit receives a synchronous signal, a clock signal and digital video data from the system (AAPA, Fig. 2 element 11);

the timing controller controls the data driving circuit and the gate driving circuit by using the synchronous signal and the clock signal from the interface circuit (AAPA, Fig. 2 element 12),

wherein the data driving circuit supplies the digital video data to the liquid crystal panel and the gate driving circuit supplies a scan pulse to the liquid crystal panel (AAPA Fig. 2 elements 13-15).

Regarding **Claim 22**, the AAPA teaches a method for supplying a power to a liquid crystal display, having an interface circuit, a timing controller, a data driving circuit and a gate driving circuit for processing digital signal, (AAPA, Figs. 2 and 4) comprising the steps of:

providing a first power source voltage from a power source of a system wherein the first power source voltage is 3.3V (AAPA, Figs. 2 and 4 VCC);

supplying the first power source voltage having a constant level of 3.3V to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit for processing digital signal of the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit (AAPA, Figs. 2 and 4 VCC elements 11-14);

generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH, and a gate low voltage VGL from the first power source voltage of 3.3V using a DC-DC converter, (AAPA, Fig. 2 element 16),

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit (AAPA, Fig. 2 element 13), and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit (AAPA, Fig. 2 element 14).

The AAPA fails to teach a second power source voltage as claimed. Tsutsui does, however, teach a second power source voltage having a constant voltage level of less than 2.9V generated from the first power source voltage using a reducing circuit, the second power source voltage being used to process digital signal of the digital circuit devices and lower than the first power source voltage, and supplying the second power source voltage to the digital circuit devices (Tsutsui Figs. 2 and 7 VDD2 is supplied as driving circuitry). A person of ordinary skill in the art upon analysing Tsutsui would have reasonably used any voltage values that are appropriate for different loads, including voltages less than 2.9V. The exact voltage values used are dependent on the voltage that is required to drive the load and are completely arbitrary, and therefore it would have been obvious to try voltages less than 2.9V along with low power loads to

achieve the predictable result of power conservation. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the power saving power supply of Tsutsui in place of the generic power supply of the AAPA in order to reduce power consumption.

Regarding **Claim 27**, the AAPA teaches a method for supplying a power to a liquid crystal display, having digital circuit devices including an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal, (AAPA, Fig. 2) comprising the steps of:

providing a power source voltage from a power source of a system wherein the first power source voltage has a constant level of 3.3V (AAPA, Figs. 2 and 4);

supplying the power source voltage to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit (AAPA, Figs. 2 and 4 VCC elements 11-14);

generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH, and a gate low voltage VGL from the first power source voltage of 3.3V using a DC-DC converter, (AAPA, Fig. 2 element 16),

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit (AAPA, Fig. 2 element 13), and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit (AAPA, Fig. 2 element 14).

The AAPA fails to teach that the power source is less than 2.9V. Tsutsui does, however, teach a similar power source, while in the power saving mode a *constant* low

level voltage is provided without variation, used for the same function that is less than 3.1V (Tsutsui, Fig. 3 element 300 and power save control signal). A person of ordinary skill in the art upon analyzing Tsutsui would have reasonably used any voltage values that are appropriate for different loads, including voltages less than 2.9V. The exact voltage values used are dependent on the voltage that is required to drive the load and are completely arbitrary, and therefore it would have been obvious to try voltages less than 2.9V along with low power loads to achieve the predictable result of power conservation. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the power saving power supply of Tsutsui in place of the generic power supply of the AAPA in order to reduce power consumption.

Regarding **Claim 32**, the AAPA teaches a method for supplying a power to a liquid crystal display, having an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signals (AAPA, Fig. 2), comprising the steps of:

providing a first power source voltage from a system wherein the first power source voltage is 3.3V (AAPA, Figs. 2 and 4 VCC);

supplying the first power source voltage of 3.3V to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit for processing digital signal of the data driving circuit and the gate driving circuit (AAPA, Figs. 2 and 4 VCC elements 11-14);

generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the first power source of 3.3V using a DC-DC converter (AAPA, Fig. 2 element 16); and

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 to the data driving circuit and supplying the gate high voltage VGH and a gate low voltage VGL to the gate driving circuit (AAPA, Fig. 2 element 14).

The AAPA fails to teach generating and supplying a second power source as claimed. Tsutsui teaches different power sources used for different parts of the display including the timing control circuitry and the driving circuitry, specifically:

generating a second power source voltage having a constant level of less than 3.1V from the first power source voltage of 3.3V using a reducing circuit (Tsutsui, Figs. 1 and 3 elements VDD1, VDD2 and VDD3);

supplying the second power source voltage less than 3.1V circuits other than the data and gate drivers (Tsutsui, Figs. 1 and 3 elements VDD1, timing controller).

With regard to the second power source voltage having a constant level of less than 2.9 V, a person of ordinary skill in the art upon analyzing Tsutsui would have reasonably used any voltage values that are appropriate for different loads, including voltages less than 2.9V. The exact voltage values used are dependent on the voltage that is required to drive the load and are completely arbitrary, and therefore it would have been obvious to try voltages less than 2.9V along with low power loads. Additionally, it would have been obvious to one of ordinary skill in the art at the time of

the invention to use the power saving power supply of Tsutsui in place of the generic power supply of the AAPA in order to reduce power consumption.

Response to Arguments

Applicant's arguments filed July 3rd 2008 regarding Claim 22 have been fully considered but they are not persuasive.

Regarding Claims 5, 18, 20, 22, 27 and 32, the applicant argues that the prior art fails to teach a "power source voltage has a constant level of less than 2.9V" or a similar limitation in all claims. The examiner respectfully disagrees. Tsutsui clearly teaches that during the power saving mode, the voltage stays constant at 3.0V, it is considered consistent with the claims because the power supply will not *always* be providing a constant voltage, for example when it is turned off, or for example if there are unforeseen electro-magnetic variations. Also the applicant argues that Tsutsui fails to teach a voltage less than 2.9V. The examiner does not contend this fact, however Tsutsui clearly gives 3.0V as the reduced power saving mode merely as an example, to have this power saving voltage be lower and higher is merely just a design choice depending on the types of circuits that are dependent on this particular power supply voltage. But the main concept of the invention is that a DC-DC converter can be used to reduce an input voltage in order to save power, the specific voltage to which the DC-DC converter drops the input voltage is completely arbitrary.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571)272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Ke Xiao/
Examiner, Art Unit 2629